

1.1 SILICON

August 1999

1.1 Subsystem Manager's Summary

Murdock Gilchriese (Lawrence Berkeley Lab.)

1.1.1 Pixel System

Costs are within allocated amounts. The first prototype disk support ring was delivered and measured at LBNL. The location of mounting holes was found to be outside specifications but the ring will still be used to assemble the first full 12-sector prototype disk. The design of the 2nd prototype ring has started and will incorporate the lessons learned from the first prototype. ESLI continues to delay shipment of the final five sectors needed for a complete disk to attempt to meet planarity specifications. The last sector is now not expected until the end of September. Allcomp, Inc completed the first phase of their contract to fabricate a prototype disk region support frame. In order to attempt to maintain the schedule on this, we have given them the go ahead to fabricate all eight panels need for phase III of there work, while in parallel the fabrication of the joint region between panels(phase II) proceeds. A 2.5 day meeting was held at LBNL to go over all aspects of the mechanical design and near-term testing, and to begin preparations for the Estimate to Complete. Concerns about fault conditions of the cooling system and interfaces remain and will be discussed at the September ATLAS meetings. It has been made clear to the pixel and ID managements that these concerns need to be resolved by the end of the year or there will be delays in our schedule. Work has started on the long optical exposure tables needed to make custom copper(later aluminum) on kapton cables.

The completion of the 2nd prototype sensors has been delayed by about five weeks by one of the two vendors, but first wafers are expected in early October (2-3 weeks behind our schedule) and can be evaluated quickly. The impact of this on the Final Design Review schedule will be assessed in September.

The FE-D submission was made to Temic on August 10 and fabrication is expected to be completed by about October 15. In addition to FE-D, other test chips, including opto-link chips designed in part by Ohio State, were included in this run. Work has started on the Honeywell version of the front-end chip, FE-H. The agreements needed to allow European's access to the Honeywell design rules are still working their way through the system and are expected to be in place by mid-October. Work has started on the onerous process of getting export license agreements for the Honeywell chips. Partly as a result of the SCT IC experience, it has been realized that our IC test system must be improved. The initial conceptual design of such a system is complete but engineering manpower is in short supply and the required talent is currently working on the RODs. We are attempting to add manpower to the ROD effort to free up immediately an experienced engineer to do the detailed design of the pixel IC test system, based on modifying the existing system.

Four panels containing eight flex circuits were delivered by CERN. Of the 32, only 14 were claimed by CERN to be good. In part this is the result of using different personnel for fabrication at CERN and it is expected that no charge will be made for this run. A second run has been initiated with more experienced personnel and better control. In addition to poor yield, we have found even "good" circuits to be of very poor quality, particularly for wire bonding. It is not clear if this run will be usable at all. R&D Circuits in the US has had numerous problems manufacturing these parts and have essentially moved now into R&D mode. If they are successful, we will go ahead with fabrication but otherwise cancel the contract. A decision will be made in December. In the meantime, another company, Compunetics, has been identified and visited and looks promising. An order for 50 flex will be placed with them with delivery 4 weeks ARO promised. The absence of good flex hybrids jeopardizes entirely the September test beam run.

The design and fabrication of tooling for module assembly advanced in August. Simple tooling for prototype assembly was completed and more sophisticated tooling aimed at production is under fabrication. An initial conceptual design for tooling and procedures needed to attach modules to disk sectors was completed. A bumped wafer from Alenia was successfully thinned to about 150 microns and diced. Additional practice wafers are still under fabrication in Germany. Lab tests of the existing flex module continued to understand problems seen in the test beam with the MCC operation and these seem to have identified MCC problems that will be discussed with the Genoa design team. Progress continues at Ohio State to develop an alternative optical package.

1.1.2 Silicon Strip System

Corrections to the bug in the ABC chip found after submission have been corrected and a new layout is complete. However, simulations are on hold because of the need to test the existing ABC wafers and chips. A waiver was granted to Honeywell and all ABC wafers delivered, after Honeywell provided test data up to 25 Mrad showing all relevant parameters were in spec. Wafers were sent to RAL for probing. Chips from the one wafer delivered to LBL were tested with good results. A single-sided module (6 CAFE and 6 ABC chips) was built and preliminary tests indicate good (prerad) performance. A double sided module is under fabrication. The new CAFE-P probe card was finally delivered and it appears functional although there are some shorts that need repair. The first part of the high-speed test system for ABC/ABCD was delivered to LBNL and is being debugged.

The news is even better on the ABCD front. Single-sided modules have been built with both variants of the ABCD (ABCD2T with trim DACs in each channel and ABCDNT without these) and both function reasonably well. However, there is a bug in the trim DAC circuitry that is understood, but which makes it impossible to trim a few channels. It was decided to buy the additional six wafers from the original ABCD run, although the second run is expected to be delivered in mid-September. The availability of more ABCD chips sooner will advance the hybrid evaluation and selection program. A final hybrid type is also planned to be selected by early December and the choice made between ABCD and CAAFE/ABC. So far it appears this can be done within funds already allocated since the acceleration payment planned for Temic is claimed now not to be required for the second run. Double-sided ABCD modules are under fabrication at RAL.

The next major step in the IC evaluation program is to understand the performance after irradiation. ABCDs have been irradiated at the PS to the equivalent of 10 Mrad and continue to function. Similar irradiations of CAFE-P and of Maxim and DMILL tests structures were done and results are expected in early September. Irradiations are also planned in October at LBNL. The bottom line of all of this is that we appear to be on track to make an IC vendor choice on schedule in early December.

Negotiations with Temic and Honeywell continued very slowly under the auspices of the Frame Contract. The major hangup is to get agreement from both on the nature of a yield guarantee for production orders. It appears that we are close to convergence with Temic, since these negotiations started first, but not yet with Honeywell, which has been slow in responding.

Revised prototype hybrids are on schedule for delivery in early September. Module fabrication tooling and procedures are in place to make the few modules needed for IC evaluation. Dummy module fabrication continues. Substantial progress has been made on the clean rooms at LBNL for SCT and pixel module production assembly. This continues to be on track for completion by early October.

1.1.3 ReadOut Drivers

The off-detector electronics group was to update their models and interfaces to the ROD. This has not been as complete as desired. A new workshop will be held at CERN the week of September 20th . One of the aims of the workshop will be to show updated models and schedules that will be placed on the web.

Work continues on the ROD. The VHDL code for the decoder (now named the formatter) is nearing completion. The ROD model has been updated and redrawn to guide the designers. The requirements need updating. These changes will be incorporated into the requirements document, under change control procedures that give estimates of cost and schedule impact along with the clear description of the changes. The simulation software effort of the SCT and pixels continues. Testing of the DSP software is on going.

Much progress has been made on the ROD. This progress needs to be reviewed. A review date has been set for about November 15, 1999. At that time it is expected that the schematics, VHDL (FPGA code) and software will be very near completion. The review group will have both ATLAS and US ATLAS representatives and will be chaired by Abe Seiden. This review is very important, for it will be an opportunity for the community to confirm/correct the design.

1.1.1 Pixel System

Milestone	Baseline	Previous	Forecast	Status
Internal Progress Review #2	15-Dec-99	15-Dec-99	1-Mar-00	Delayed (See #1)

Note #1 Review will become part of Estimate to Complete review.

1.1.1.1 Mechanics

1.1.1.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Complete fab 1st prototype ring	1-Apr-99	30-Jun-99	15-Aug-99	Completed
Complete frame Phase I	1-Jul-99	1-Jul-99	15-Sep-99	Delayed (See #1)
Complete fab 1st prototype disk	1-Jul-99	1-Jul-99	15-Oct-99	Delayed (See #2)
Select Sector Baseline Concept	1-Sep-99	1-Sep-99	15-Dec-99	Delayed (See #3)
Sector PDR	1-Sep-99	1-Sep-99	1-Feb-00	Delayed (See #4)
Module Attach CDR	1-Sep-99	1-Sep-99	25-Sep-99	Delayed (See #5)
Complete frame Phase III	1-Feb-00	--	1-Feb-00	On Schedule

Note #1 Original honeycomb for panels was not adequate and new honeycomb was ordered, causing delay

Note #2 Sectors from ESLI have been delayed.

Note #3 Need revised cost estimate and other technical information.

Note #4 Prototype disk delays and lack of complete information on all aspects of sectors(including costs).

Note #5 Pixel week was moved to week of Sep. 20.

Murdock Gilchriese (Lawrence Berkeley Lab.)

Design studies by Hytec, Inc for the overall pixel support frame continue. The corner block details of the overall support frame panels have

been modified to include two alignment pins with the objective of bonding an octagonal frame to final dimensions that does not require machining. Calculations were made by Hytec of the out-of-plane deflection of the first prototype disk support ring to compare with measurements. Design of the second stage of prototype disk support ring was begun by Hytec.

1.1.1.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Testing of 5-Disk Protos	1-Sep-99	1-Sep-99	15-Dec-99	Delayed (See #1)
Complete frame Phase II	1-Oct-99	1-Oct-99	1-Nov-99	Delayed (See #2)
Compl Testing of Disk Prototypes	21-Dec-99	21-Dec-99	1-Jun-00	Delayed (See #3)
Complete frame Phase III	1-Feb-00	--	1-Feb-00	On Schedule

Note #1 ESLI delays and more information needed to make final selection

Note #2 Phase I delays push back Phase II

Note #3 Rescope testing program to include more testing of disks including mounts and insertion tooling

Murdock Gilchriese (Lawrence Berkeley Lab.)

ESLI, San Diego, has delivered 3 more sectors, for a total of 7, of the planned 12 prototype sectors to be used in fabricating the first

prototype pixel disk. The delivery of the remaining 5 sectors has been significantly delayed in an attempt to improve the planarity of the sectors.

The first 7 sectors have good general appearances and the weights indicate acceptable average radiation lengths. However of these first 7

sectors, 3 meet our planarity requirements and 4 do not. The 4 that do not are still useful for a prototype disk. The planarity problem,

reported last month, has been further discussed with ESLI. The delayed delivery of the remaining sectors is the primary reason for the delay in

assembly of the first prototype disk and selection of sector baseline concept.

The prototype disk support ring, the support for the above ESLI disk sectors, has been received by LBNL. CMM measurements of the

sectors locating holes have revealed deviations of up to 0.5 mm in hole locations. This is unacceptable; however use can still be made of this

support ring for structural studies which was the original purpose of the first prototype disk. The reason for the misplaced holes is believed due

to drill wander when drilling carbon fiber materials. Also the out-of-plane deflections due to applied force have been preliminarily measured.

These are greater than desired and will lead to support ring redesign.

Parts have been fabricated for prototype number 5 of the aluminum tube sector design. This sector is designed to reduced the out-of-plane

distortion due to coolant pressure of prototype number 4.

A 1 KW chiller (at -20 degrees C) has been order to test the prototype disk at operating temperature and power. Pressure and flow

measuring devices for the prototype disk have been received. Data logging electronics has also been ordered.

The phase 1 global support panels have been lightweighted with holes of proper shape and returned to Hytec for TV Holography testing. The results will be compared to tests before lightweighting. Corner splices for the global panels of phase 2 have been successfully molded. Tooling for the first corner tubes has been made. Material for the corner blocks of the panels has been received. Thick laminates will be constructed in order to machine the corner blocks.

1.1.1.2 Sensors

1.1.1.2.1 Design

Sally Seidel (University Of New Mexico)

Small changes were made to the Second Prototype sensor masks to accommodate production requirements at the vendors.

1.1.1.2.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Fabr of Second Protos	21-Sep-99	21-Sep-99	1-Nov-99	See Note #1

Note #1 This delay is not expected to impact the prototype module assembly schedule due to the fast turnaround provided by the 4 institutes that characterize the wafers.

Sally Seidel (University Of New Mexico)

A yield analysis on First Prototypes with normal and moderated p-spray was conducted on the basis of their breakdown voltages. Masks for the Second Prototypes were sent for fabrication following small changes necessary to adapt them to the production process of the vendors. Receipt of Second Prototypes is expected to begin in early October and conclude in November. Organization of the FDR and the PRR proceeded. US-ATLAS members participated in the CERN beam test where single chip and tile assemblies were studied. A new revision of the PixelDAQ software was downloaded at sensor and module testing institutes in preparation for Second Prototype tests.

1.1.1.2.3 Production

Sally Seidel (University Of New Mexico)

A new technician (T. Palmer) began training in sensor probing and DAQ system operation at UNM. He and G. Santistevan will be the principal technicians responsible for probing Second Prototype, pre-production, and production sensors at UNM.

1.1.1.3 Electronics

1.1.1.3.1 Design

Milestone	Baseline	Previous	Forecast	Status
Complete design of HSOI test die	16-Apr-98	16-Apr-98	1-Nov-98	Completed
Comp. Des. Honeywell Rad-Hard Test Dev	16-Apr-98	--	16-Apr-98	Completed
Complete fab HSOI test die	26-Aug-98	26-Aug-98	31-Mar-99	Completed
Complete design DMILL test device	15-Dec-98	--	15-Dec-98	Completed
Submit Honeywell SOI test die	15-Jan-99	--	15-Jan-99	Completed
Final Des. Rev. DMILL Rad-Hard Proto	25-Jan-99	25-Jan-99	21-Jul-99	Completed
1st design review of DMILL proto	25-Jan-99	25-Jan-99	23-Feb-99	Completed
Comp Design DMILL RAD-Hard proto	26-Feb-99	26-Feb-99	10-Aug-99	Completed
Final design review Honeywell 1st Proto	5-Mar-99	5-Mar-99	1-Feb-00	Delayed (See #1)
Comp des. Honeywell FE Rad-Hard Proto	2-Apr-99	2-Apr-99	15-Feb-00	Delayed (See #2)
Comp. fab DMILL test device	30-Apr-99	30-Apr-99	15-Oct-99	On Schedule

1st design review of Honey. Proto	1-Jun-99	1-Jun-99	1-Dec-99	Delayed (See #3)
Comp. eval.HSOI test die	1-Jul-99	1-Jul-99	1-Dec-99	Delayed (See #4)
Comp. eval.DMILL test device	1-Jul-99	1-Jul-99	1-Aug-99	Completed

Note #1 Decision to pursue DMILL and HSOI sequentially, followed by significant delays in DMILL prototype submission have generated significant delay here.

Note #2 Same as above

Note #3 Same as above

Note #4 Relocation of critical design engineer in Geneva, and resulting need to use commercial IC tester for testing have led to significant delays in the characterization of this chip.

Kevin Einsweiler (Lawrence Berkeley Lab.)

After a few last minute technical problems, the FE-D DMILL submission was finally made to TEMIC on Aug. 10. Final Verilog verification was done using a complete collection of standard test vectors, and final SPICE simulations were done as well. The latter were performed for a complete 320 pixel column pair with 24 End-of-Column buffers (and all circuitry at the bottom of the chip) as well as for a "chopped" schematic containing 18 columns of 16 pixels length and 4 EOC buffers per column pair. The former simulation is about 55K transistors and the latter about 85K transistors. The SPICE simulations were done for 3V pre-irradiation operation, as well as 4V 25 MRad "end of lifetime" operation. Operation at full readout speed with no errors was observed in all cases, including operation of column data transfers at 20 MHz.

The complete reticle for this TEMIC DMILL engineering run was built up in Bonn to insure that the geometry of the layout is exactly what we want. The reticle includes two pixel array chips (FE-D). These chips contain about 200 probe points around the chip border to allow more detailed characterization and debugging as necessary using Picoprobes. In order to assist in the characterization of the modified front-end design included in FE-D, a small analog test chip has also been included in the reticle, including examples of all of the analog circuitry in the full pixel array. This encompasses the current reference, the current and voltage mode DACs and their control registers, the internal bias generation circuitry, as well as the charge injection circuitry. This small array allows evaluation of the front-end performance with known capacitive loads and controlled leakage current injection, as well as observation of internal nodes in the front-end. The reticle also includes an MCC prototype from Genova containing many improvements towards a final version, but not yet representing a complete chip. It does contain all of the major functional blocks to allow evaluation of performance, and also includes large I/O pads to investigate different attachment schemes for the Flex hybrid, including TAB bonding. There are also prototypes of opto-link chips (all CMOS versions of the DORIC receiver chip and the VDC VCSEL driver chip). The opto-electronics designs are based on those of the SCT, but have been transferred from a commercial rad-soft bipolar process to DMILL by Siegen and Ohio State University. A special process monitor bar has been developed by LBL to allow reliable extraction of SPICE models from the FE-D wafers so that we can cross-check our design performance against expectations. Finally, a rad-hard LVDS buffer is included which will allow us to make a complete rad-hard version of the single-chip support card that we use for testing single chips in the lab and testbeam. With this buffer, we have the capability to operate a single pixel chip (or electronics/sensor assembly) while it is being irradiated to LHC fluences. In all, there are 10 separate die included in the roughly 15x15mm reticle, and we expect to get about 57 good reticles per 6" wafer, and a minimum of eight wafers delivered from this run, giving us roughly 1000 potentially good pixel array die.

We have arranged to accelerate the fabrication time to roughly 9 weeks instead of the usual 12, in order to get results as quickly as possible from the submission. Hence, we expect to be testing these new wafers in our labs roughly around Oct. 15. We already have appropriate wafer probing capability set up in our lab for testing these chips, but we will be upgrading the corresponding software over the next few weeks in order to be fully ready when the wafers return. The probing is likely to be divided between Bonn and LBL, and we have also supplied Bonn with an appropriate interface card, and some chip testing software. We have made a first pass through the modifications and improvements made since our previous front-end chips (FE-B and FE-C), as well as all bit definitions and operational subtleties involved in operating the new FE-D chips, in order to prepare a list of software changes (and some minor firmware changes to the PLL). We are presently working on an updated list of tests and characterizations to perform during initial FE-D testing, and we expect the necessary firmware and software changes to be in place prior to the return date of the wafers.

Now that the DMILL pixel array is in fabrication, we have returned to preparing for the Honeywell SOI pixel array design (FE-H). We are continuing to work on improving the technology file and design rules we have received from Honeywell for Cadence (they clearly do not have other customers who do significant amounts of full-custom design). This is progressing well, but there are some uncertainties about the new "simplified design rules" which Honeywell has created in order to address State Dept. concerns related to export control. It seems to us that certain critical design information is not provided in the new set of documentation, and we are discussing these aspects with Honeywell.

A preliminary list of design goals for the FE-H chip has been created, and will be refined over the coming few weeks. The new design will start from the schematics for the DMILL FE-D chip, and should require fairly minor modifications. Several improvements will be possible, including improved design for the hit logic in the pixel back-end (to cope better with multi-hit situations) as well as improvements in the RAM cells in the pixel. The RAM design for DMILL was extremely constrained by size and wiring limitations, and we barely managed to achieve acceptable performance by using bipolar sense amplifiers at the bottom of the columns to recover the transmitted data. In HSOI, it will be possible to return to an NMOS-based RAM design, and we expect greater performance margin, and a simplified sense amplifier design. Another major goal for the HSOI chip is to push the pixel cell size and EOC buffer size down as far as possible. We expect that this will lead us to a 300 micron pixel size, and at least 30-32 EOC buffers, both of which we believe are necessary to achieve our performance goals in the B-layer. The improved routing capabilities in HSOI should also allow us to shrink the region required for the other support logic in the bottom of the chip. This is probably essential for reducing the size of the "dead" peripheral region from the present 2.8mm to the production design goal of 2.5mm, without giving up large numbers of EOC buffers.

The next steps will be to create the equivalent standard cell infrastructure we used for FE-D (a large library of standard cells with schematic and Verilog views, all characterized at the SPICE level for delay and drive performance). This allowed us to create very coherent and readable schematics which automatically provided a detailed Verilog simulation of the entire chip, including annotated delays for the corner models. These simulations in turn were a significant part of our design verification procedure. By actually creating the corresponding layout views as well, we would have a library that could be used in synthesizing an HSOI MCC chip if necessary. With this infrastructure in place, real layout work on the pixel back-end and EOC buffers can begin on a timescale of early October.

In order to exercise the next generation of chips from TEMIC and Honeywell to the fullest extent possible, and in particular to develop the capability to label chips as "known good die", and be sure that this classification will remain true after exposure to the full radiation doses of ATLAS, we are developing an improved test system. This system uses many of the same techniques present in commercial IC testers, but applies them in a focussed way to the specific chip testing problem that we have. We believe this is

essential to do parametric testing of certain parts of the chip (modified clock frequencies, power supply voltages, and signal phasing), and evaluate for each die how far away they are from our specifications. Many chips would then be characterized before and after irradiation. This will allow us to develop "strict selection criteria" which a chip should pass before irradiation, in order to be sure that it would pass "standard selection criteria" after irradiation. The initial conceptual design of this system is complete, and we hope to complete the detailed schematics over the coming two months, in order to have working boards by late Fall this year. This system will be critical for evaluating our upcoming rad-hard pixel chip submissions, and arriving at the optimal final chip design and vendor for ATLAS late in 00. We are presently trying to find enough engineering manpower to complete this design work without significant impact on the local SCT/pixel ROD design effort.

The new test system will also allow us to perform more sophisticated production testing than presently possible with our PLL test system. By using this new system to test larger numbers of modules in the next 6-9 months, before and after irradiation, we expect to derive the detailed list of tests required at each step in the module serial production, including a first pass at a burn-in protocol. This will allow us to decide which test steps need the performance of the more complex test system (elevated speed and parametric testing) and which can be performed with the existing test system, and what minor additional hardware will need to be designed. This process would then lead to final optimization of the electronics test capabilities of the production sites late next year, in preparation for startup of serial production in 2001.

Richard Kass (Ohio State)

Ohio State

We are currently preparing for the test of the radiation hard version of the DORIC4 chip that we expect to receive in October. We have received the electronic module used by Rutherford to generate the bi-phase marked clock and a tested radiation-tolerant DORIC4A chip. We need to construct a module to house the DORIC4A chip and connect it to the module that generates the bi-phase marked clock. The plan is to fully understand the testing of DORIC4A so that we are ready to test the rad-hard DORIC4 when it is delivered.

1.1.1.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Fabr of Honeywell Sol Test Devices	26-Aug-98	1-Mar-00	31-Mar-99	Completed
Compl Fabr of DMILL Proto	23-Jul-99	--	15-Oct-99	On Schedule
Compl Fabr Honeywell Protos	25-Aug-99	--	1-Jun-00	Delayed (See #1)
Compl Testing DMILL Prototype	9-Dec-99	1-Jun-00	15-Jul-00	Delayed (See #2)
Review Design Approach	19-Jan-00	19-Jan-00	1-Aug-00	Delayed (See #3)
Compl Testing Honeywell Prototype	15-Feb-00	15-Feb-00	15-Jul-00	Delayed (See #4)
Vendor Selection	29-Feb-00	29-Feb-00	15-Aug-00	Delayed (See #5)

Note #1 Significant delay in DMILL prototype has delayed forecast Honeywell prototype submission date

Note #2 Completion of testing delayed to match Honeywell schedule

Note #3 Same as Note 1 above

Note #4 Same as Note 1 above

Note #5 Same as Note 1 above

LBNL

The Honeywell SOI multi-project submission which we made in Nov. 98 has returned to LBL and undergone preliminary evaluation. A test program written by our engineer for the CERN IC tester in Geneva is now working, and has provided additional test data. However, due to limited access to this test equipment (conflicts with ABCD testing for ATLAS SCT), and due to the limited capability of the IC tester analog hardware, it has proven very difficult to complete the characterizations as we had wanted. The designer of the HSOI test chip will therefore return to LBL for a limited period in early October to complete characterization work using our existing LabView-based test setup. We expect to have fully tested several test chips and several test structures by mid-October, and plan to irradiate them in a run at the 88" cyclotron in late October. We have also received corner models for the HSOI process from Honeywell, which we have compared to our previous test structure measurements. We find the Honeywell models to be more pessimistic than our measurements, as expected for 3-sigma corner models.

1.1.1.4 Hybrids**1.1.1.4.1 Design**

Milestone	Baseline	Previous	Forecast	Status
Compl. Design of 1.x proto	1-Apr-99	--	21-Apr-99	Completed
Select Hybrid Type	15-Apr-99	[New]	15-Apr-99	Completed
Design of Prototype 2.0 Begins	1-Sep-99	[New]	1-Sep-99	On Schedule

Rusty Boyd (University of Oklahoma)

Efforts continue to define the mechanical parameters of the assembled flex hybrid module. M. Gilchriese has begun a controlled document listing the values as they are presently understood. Still at issue are the values required to properly decouple the front end chip power supplies. Since this cannot be known absolutely until the final electronics are delivered, we propose to investigate decoupling capacity vs. mechanical cost. It is fairly certain that all the filtering required for the 80 m of power lines coming into the module cannot be accomplished on the Flex Hybrid. Additional decoupling will most likely be required at connection points such as PPB1. This should be a much more realistic approach to the problem, since we need to freeze the mechanical parameters soon.

We have hired an EE graduate student to replace the one who graduated last month. He will be continuing the simulation and testing program begun by his predecessor.

1.1.1.4.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Fabrication of 1.x Complete	1-Aug-99	[New]	15-Oct-99	Delayed (See #1)
Singulate Prototype 1.x Complete	15-Aug-99	[New]	15-Oct-99	Delayed (See #2)
Assembly of Prototype 1.x Complete	1-Sep-99	[New]	15-Dec-99	Delayed (See #3)
Module Assembly with Prototype 1.x complete	15-Sep-99	[New]	15-Sep-99	On Schedule
Prototype 1.x tests complete	15-Oct-99	[New]	1-Feb-99	Delayed (See #4)

Note #1 R&D Circuits will not be able to deliver v1.x Flex Hybrids. CERN was late for unknown reasons. Fabrication with Compunetics is pending.

Note #2 Singulation will proceed when final batch of CERN flex circuits is delivered (ETA = 15-Sep-99). It is expected to take about 4 weeks to singulate at Spectralytics.

Note #3 Delivery of the last 1.x prototypes from Compunetics is not expected until mid-October, 1999 (they will be singulated there). Different decoupling schemes will be evaluated and so assembly will be staggered.

Note #4 Tests will continue until delivery of prototype 2.0 Flex Hybrids are received.

Saj Alam (SUNY Albany)

Our VME setup is now working with the PLL and PCC. We now have all equipment in hand to test modules except a module itself.

The probe card to probe the front end chip wire bonding pads on the Flex Hybrid is here, as is the probe card holder, and both have been installed on our probe station. The probe card was designed to our specifications. We (Albany and OU) are determining the interface to the OU VAMUX chip to multiplex the 35 channels from the probe card, thus to measure resistances.

We are also currently working on microprobe-based testing of one of the failed new flex circuits from CERN.

Rusty Boyd (University of Oklahoma)

Thirty-two un-singulated v1.1 Flex Hybrids in four panels were delivered in late August. Two panels were delivered to UOK, one to LBNL and one to Genova. Of the thirty-two circuits, fourteen are reported by CERN to be without defects (most of these were good only after repair at CERN). Another nine panels were started immediately, before receipt and evaluation of the first batch. Singulation will proceed when all flex circuits are received. For now, the labs are cutting them out of the panels by hand. Unfortunately, a few bond pads on some the reportedly good flex circuits are contaminated by an unknown substance. We will attempt to clean these.

There are other problems with the fabrication, also. The four holes in each corner for spotting the alignment fiducials on the sensor are not 0.5 mm as specified (they appear to be the same size as the vias). In addition, the 1 mm via hole for the bias connection to the back of the sensor is not drilled through the bottom cover layer. These two problems can probably be corrected when the flex circuits are singulated. LBNL has reported some bond pad delamination. They have been able to work around this problem so far by making the flex bond second, so that there is less pull force exerted on the pad.

The personnel at CERN also neglected to include the test structure on each of the panels. This makes characterization of the process much more difficult for us. Rusty Boyd will discuss these problems with them while there in September for the Pixel meetings.

We have begun assembly of two good CERN v1.1 Flex Hybrids. One will be used to build a module at UOK. The other will be sent, along with an unassembled, defective v1.1 flex, to Bonn for module assembly development.

R&D Circuits continues to have difficulty producing flex circuits. They have succeeded in laser drilling all the holes, but are now having difficulty laying the pattern for the traces. This has essentially become a research and development project for them, and will take several months, at least, to complete. We plan to leave the purchase order in place with them at least through December, 1999 and reevaluate their progress at that time. If and when fabrication is completed with R&D, it will most likely be with v2.0 or 2.x Flex Hybrids.

A purchase order to Compunetics (Monroeville, PA) is winding its way through our purchasing system at this time. We plan to have them proceed with fabrication as soon as we are able to evaluate the CERN flex for layout errors and generate corrected drawings.

The expected delivery date is 4 weeks after receipt of the final drawings.

1.1.1.5 Modules

1.1.1.5.1 Design

Milestone	Baseline	Previous	Forecast	Status
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2nd Prototype Design Review	17-Sep-99	10-Sep-99	25-Sep-99	Delayed (See #1)
Compl 2nd Proto Design	14-Oct-99	14-Oct-99	15-Feb-00	Delayed (See #2)

Note #1 P1xel week meetings were moved to week of September 20 and expect review to be in these meetings

Note #2 Results from expanding the scope of 2nd prototype design to be more like the expected actual modules rather than an evolutionary step from the 1st prototypes.

Murdock Gilchriese (Lawrence Berkeley Lab.)

The design of module assembly fixtures advanced to include the completion of shop drawings for the manufacture of a custom vacuum chuck to hold a loaded flex hybrid, manipulate it for dispensing glue and then to mount it on a module. Fabrication is expected to be completed in September. The design of a glue-dispensing station was completed and the fabrication of some parts began. Again, completion is expected in September. A proposed module assembly sequence was agreed to but must be validated by trials. This activity is intended to develop the methods for production assembly and to assist in assembly of the new few prototype modules. In order to assemble a few modules for the September test beam run, simpler fixtures were designed that rely on "by hand" positioning and adhesive dispensing. The design of these simple fixtures was completed and fabrication will be complete in early September.

The initial conceptual design for attaching modules to disk sectors was completed. Detailed design of prototype stencils/masks for screening on adhesive and fixtures to reference the modules to sector alignment marks began. One or more dummy sectors will be fabricated to test these concepts. Dummy silicon pieces have been cut to the correct size and defective flex hybrids will be attached to these pieces, and then these assemblies attached to sectors to test the design. Fixtures should be ready by mid-October to begin these tests.

1.1.1.5.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Tests of First Protos	18-Mar-99	17-Sep-99	15-Feb-00	Delayed (See #1)

Note #1 Results from expanding the scope of the 2nd prototypes and delays in the fabrication of 1.x hybrids that have delayed lab tests and will allow (we hope) one test beam run to be completed by end September 99.

Kevin Einsweiler (Lawrence Berkeley Lab.)

LBNL

We finally received two new identical multi-chip module assemblies from IZM in late August. We are presently assembling these as two Flex modules for the Sept H8 testbeam period. The modules will use the new Flex 1.1 fabricated by CERN. These Flex were recently delivered, and were unfortunately fabricated when a critical person was absent from CERN, so their yield and quality is poorer than usual. We have also observed adhesion problems between the copper traces and the Kapton substrate when wire-bonding, but it appears that with careful treatment, it is possible to assembly a module with these Flex. One of the most critical problems in defining the Flex module envelope, and the MCM-D module design is the required number of passive components, in particular the decoupling capacitors required to achieve stable and low noise operation of a module. For this reason, we are building up two Flex modules in parallel which are identical except for the decoupling capacitors. For one module, we are systematically using the smallest components we could find (0402 ceramics and 0603 Tantalums), with realistic HV decoupling and temperature measurement (Pt1000). For the other module, we are using a

larger set of capacitors, including 0603 ceramics and 0805 Tantalums. The present Flex design has a realistic set of components for everything except the opto-link (which is not included at all), and so these tests will give us vital information. The present module envelope would not allow us to use a ceramic decoupling as large as an 0603 close to any FE die. These modules will also be mounted with the new generation of Flex support card, which includes many new features. Among those features is a provision to connect realistic power cables which are presently being fabricated by LBL (including a long low-mass portion which will connect to the support card with a Flex connector). When connected to power supplies by these prototype cables, these new modules should give us fairly clear information on what sort of passive component burden we need on the Flex in order to achieve our performance goals.

The new modules are presently being assembled, using the first generation of realistic tooling and gluing protocols from Fred Goozen at LBL. A rigid epoxy attach is being used for mounting the Flex hybrid on the sensor. Preliminary wire-bonding information indicates that this will provide adequate support under the wire-bond pads. The module assembly should be completed in the next few days, and we expect to be able to bring fully characterized modules with us to the testbeam on Sept. 18.

We have continued to study our existing Flex 1.0 module in the lab. A significant upgrade of our lab test software, to allow parallel characterization of the 16 FE chips on the module (similar to the testbeam operating mode) has been made. This requires a substantial increase in the host PC memory in order to support all of the data accumulation (256MB is needed for acceptable performance). Using this approach, we have been able to reproduce many of the MCC readout problems we saw in the testbeam in July. In particular, when reading one FE chip at a time we do not see any errors. However, when reading many FE chips at the same time, with a relatively large number of calibration hits, we do begin to see similar patterns of errors to those found in the testbeam. We have made comparison runs using the MCC chip in transparent mode (but having all of the FE chip operating in parallel) and using the MCC chip in full event building mode. This is not a perfect comparison, but strongly suggests that the errors arise during the MCC event building and are not related to the FE chip operation. Further progress on these problems requires more modules to try to confirm systematic patterns of problems, as well as additional systematic testing of the MCC chip itself in Genova using a dedicated test system which they have been building. We expect to gain better understanding after spending time with Genova experts in the September pixel week and the H8 testbeam.

These "system test" results are critical to finalizing the MCC design for the next generation submission, to be made in early 00. That chip should be very close to a pre-production version, and should be capable of reliable operation even under quite high noise conditions.

Murdock Gilchriese (Lawrence Berkeley Lab.)

Two indium-bumped wafers were delivered from Alenia for thinning. One wafer was broken in transit but about 70 die can be recovered after dicing. This wafer fragment will be used to test high-precision dicing with MTI in Ventura to compare the repeatability of die size to conventional dicing vendors. At the moment we plan to use the precision die edge on a module to place a module on a disk sector with simple tooling and then measure accurately the location of a module using an optical measuring machine(see below). We believe the precision(repeatability) attainable from normal dicing vendors may be at the edge of our placement specification and so want to try a precision(<5 micron) dicing vendor. The other wafer was successfully thinned by Okamoto in the Bay Area to about 155 microns. Tru-Si Technology also in the Bay Area successfully thinned a dummy wafer from IZM(same type of wafer previously broken by Okamoto and GDSI) using their non-contact thinning method. The defects present in the IZM dummy wafers that caused them to crack under thinning are claimed to be understood by IZM and more dummy wafers will be fabricated for delivery in late September for additional trials.

Two wafers with simple alignment marks were manufactured in the LBNL Microsystems Lab and diced to provide hundreds of small(1 mm x 1 mm) targets that may be mounted (glued) to disk sectors or other structures for optical alignment using the SmartScope system at LBNL or similar optical measuring machines. A few of these targets were mounted on a flat plate and measured. These initial measurements indicated that if multiple(three or more) measurements are made at a single point and averaged that x or y (in-plane) rms precision of 2-3 microns appears feasible and about 7-8 microns in z(out-of-plane). This is roughly a factor of two better than required. These targets will be used to reference similar targets on the module sensors and IC die to the mounting holes of disk sectors.

K K Gan (Ohio State)

Work is continuing on the design and fabrication of a prototype optical package. The procedure for depositing Au/Cr traces on the bases has been systematically investigated. We find that a minimum of ~1 micrometer of Au over ~0.1 micrometer of Cr is needed for wire bonding because the surface of macor is uneven at 10 micrometer level. This requires a long deposition time and hence we decided to explore the alternative procedure of screening on the Au. We have placed an order with Hybrid-Tek for depositing 12 micrometer of Au on up to 8 macor rods (9 bases/rod) and expect the delivery in about 3 weeks.

The VCSEL is supposed to be attached to the Au trace on the base using the surface mount technology. Several attachment attempts were not successful. We believe that this is due to the lightweight (0.007 microgram) of the VCSEL, resulting in little physical contact between the Au/Sn layer on the bottom of the VCSEL and the Au trace. A small pressure must be applied on the VCSEL. Two different jigs for applying the pressure were fabricated. One uses two small custom-made needles and the other uses two small custom-made brass chips with the same dimension as the VCSEL. Both techniques failed. We are currently investigating the possibility of tinning the gold traces to even out the surface and provide more contact between the VCSEL and the trace.

1.1.2 Silicon Strip System

1.1.2.1 IC Electronics

1.1.2.1.1 Design

Milestone	Baseline	Previous	Forecast	Status
Frame Contract in Place	15-Apr-99	30-Jul-99	30-Sep-99	Delayed (See #1)
Final Design Review	3-Mar-00	--	3-Mar-00	On Schedule
Compl Spec for Preprod Release Order	3-Mar-00	--	3-Mar-00	On Schedule

Note #1 tbd

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

The corrected ABC design that fixes the bug found just after the last submission has been incorporated into a new layout which fits within the existing chip dimensions. Therefore, layout is complete and final post-layout simulations could be performed. However, people who would be involved with that are now busy testing the newly arrived ABC chips so this final simulation will have to wait. We don't anticipate the post-layout simulations including full parasitics to show any new speed problems but it will need to be completed before any new fabrication is ordered should that be decided at the December review of the two readout options.

The probe card for full 128-channel CAFÉ-P testing was delayed again during August as the vendor had more trouble than expected in aligning all the probe pins. The card was received just at month end. Initial checkout shows that it is working, however, some pins, which probe outputs of the CAFÉ-P, are shorted together. By ignoring the shorted channels, we are continuing to checkout the test system and card. We will decide soon whether we will test the two CAFÉ-P wafers with the card as is in order to provide ICs

to our collaborators with unknown results on a few channels per chip or whether we will first return the card for repair. We are in discussion with the vendor as to how long the repairs will take. On the positive side, we have obtained good results with the probe card and test system, operating at 1 fC threshold. All PCBs for the new ABC tester are in-house and software is ready for rudimentary testing but work is still continuing on checkout of the system.

1.1.2.1.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Complete Fabr of 2nd ABC	19-Apr-99	3-Aug-99	18-Aug-99	Completed
Test Systems Complete	26-Apr-99	31-Jul-99	30-Sep-99	Delayed (See #1)
1st ICs Avail for 2nd Proto Hybrid	18-May-99	30-Aug-99	27-Sep-99	Delayed (See #2)
Complete Fabr of 2nd ABCD	30-Jun-99	26-Jun-99	30-Sep-99	Delayed (See #3)
Compl. metallization 1st ABCD	30-Jun-99	--	23-Jul-99	See Note #4

Note #1 TBD

Note #2 TBD

Note #3

Note #4 On hold. May not be needed.

Alexander A. Grillo (University Of Calif. At Santa Cruz)

LBNL & UCSC

Test results from CERN continue to show good performance of the new ABCD designs. Two single-sided modules were built, one with the trim-DAC version of ABCD and one with the no-trim-DAC version. The instability problems of the previous design seem to be cured. Radiation damage tests at the CERN PS show that the channel-to-channel matching of the no-trim-DAC version degrades by about a factor of 3 after 3×10^{14} protons which pushes it outside the SCT requirement. For this reason we are recommending that the no-trim-DAC version be discarded and evaluation continue of the trim-DAC version. One problem has been found with the trim-DAC design. On some channels the trim-DACs appear to create a large voltage offset which cannot be fully corrected by the DAC setting. The designers have determined that this is caused by an error in the biasing current of the transistor used to feed the trimming level into the comparator and can be corrected by increasing the bias current. This analysis is supported by the fact that after irradiation when the beta degradation causes the transistor to draw more current, this voltage offset problem decreases. The fix is still under study. According to plans, we will receive a double-sided ABCD module for testing in the US in October.

The ABC wafers have been accepted from Honeywell. We granted them a waiver of the VTN pre-rad issue discussed in last month's report. Honeywell performed further tests on the wafers showing that the VTN stayed within their post-rad spec up to 25 Mrad. LBNL has tested a few chips from one wafer and found it to be functioning up to 25 MHz at wafer probe. The chips seem to be fully functional. RAL is just getting started with testing and we have not yet received any reports from them.

One singled-sided module with CAFÉ-P and ABC chips has been built (6 chip pairs). Preliminary results show good functionality with expected noise levels and stable operation below 1 fC threshold. This module will be brought to the beam test at CERN in September. A double-sided module is now under construction.

1.1.2.1.3 Production

Milestone	Baseline	Previous	Forecast	Status
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Preliminary design review	3-Aug-98	--	15-Sep-99	Completed
Select Approach/ IC Vendor	10-Dec-99	--	10-Dec-99	On Schedule

Alexander A. Grillo (University Of Calif. At Santa Cruz)

Not very much progress was made on the Frame Contract in August, partly due to European vacations throughout the month. We are still waiting for a response from Temic to CERN's latest proposed contract. We believe this is close to finished since all open issues have been addressed but acceptance of the final wording is still required. Progress with Honeywell has been more slow. At our last meeting in August, Honeywell had made some progress on the issues resolving satisfactorily the CERN requirement for bank guarantees. However, they had made no progress on your request for yield assurance nor export licenses. They committed to make proposals on the open issues by 27-Aug but we have not received anything yet. We don't seem to be able to move Honeywell at an acceptable rate towards conclusion. We will have more discussions with CERN purchasing during ATLAS Week in September and perhaps we can close on the Temic contract but it appears Honeywell's version will be delayed beyond our target of 30-Sep.

1.1.2.2 Hybrids/Cables/Fanouts

1.1.2.2.1 Design

Milestone	Baseline	Previous	Forecast	Status
Compl 2nd Proto Hybrid Substrate Design	29-Oct-98	--	15-Jun-99	Completed
Compl 2nd Proto Fanout Design	29-Oct-98	15-Jun-99	1-Oct-99	Delayed (See #1)
Compl 2nd Proto Cable Design	29-Oct-98	15-Jun-99	1-Oct-99	Delayed (See #2)
Hybrid Final Design Review	11-Feb-00	--	11-Feb-00	On Schedule
Compl Preprod Hybrid Substrate Design	11-Feb-00	--	11-Feb-00	On Schedule
Compl Preprod Fanout Design	11-Feb-00	--	11-Feb-00	On Schedule
Compl Preprod Cable Design	11-Feb-00	--	11-Feb-00	On Schedule

Note #1 same explanation as 2nd prototype cable design

Note #2 The 2nd prototype hybrid was designed to use the existing cable from the 1st prototype design. We are holding this item for the development of a modified cable based upon upcoming test results from the 2nd prototype hybrid.

Carl Haber (Lawrence Berkeley Lab.)

No work in this area

1.1.2.2.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Proc of 2nd Proto Discrete comp.'s	11-Mar-99	--	1-Jul-99	Completed
Compl Fabr of 2nd Proto Hybrid Substrate	11-Mar-99	1-Aug-99	7-Sep-99	Delayed (See #1)
Compl Fabr of 2nd Proto Fanout	11-Mar-99	1-Aug-99	1-Dec-99	Delayed (See #2)
Compl Fabr of 2nd Proto Cable	11-Mar-99	1-Aug-99	1-Nov-99	Delayed (See #3)
Complete 2nd Prototype Assy	17-May-99	15-Aug-99	1-Oct-99	Delayed (See #4)
1st 2nd Prototype Hybrids Avail	14-Jun-99	15-Aug-99	15-Oct-99	Delayed (See #5)
Compl Test of 2nd Proto Hybrid	8-Dec-99	--	8-Dec-99	On Schedule

Note #1 There were delays at the vendor and this is the new promised delivery date

Note #2 see notes for design of this item

Note #3 see notes for design of this item

Note #4 this is the time required to assemble a set after they are received.

Note #5 this is the time required to test

Carl Haber (Lawrence Berkeley Lab.)

The 2nd prototype is in fabrication at a number of vendors. There have been delays at the vendors and they are now promised for Sept 7, 1999.

1.1.2.2.3 Production

Milestone	Baseline	Previous	Forecast	Status
Select hybrid substrate type	10-Dec-99	--	10-Dec-99	On Schedule

Carl Haber (Lawrence Berkeley Lab.)

No activity.

1.1.2.3 Module Assembly and Test

1.1.2.3.1 Design of Assembly & Tooling

Milestone	Baseline	Previous	Forecast	Status
Prototype Tooling Complete	1-Apr-99	1-Aug-99	1-Oct-99	Delayed (See #1)
Compl Fab of tooling for proto	14-Jun-99	--	15-Nov-99	Delayed (See #2)
Compl Design of Proto Mod Assy/Test Tool	14-Jun-99	--	15-Nov-99	Delayed (See #3)
Prelim Design Review of Module Assy	27-Dec-99	--	27-Dec-99	On Schedule

Note #1 the tooling design and reviews depend upon progress at a number of sites all working in parallel. Not all are up to the same level. There has also be a delay in obtaining FE electronics which has delayed the evaluation of modules.

Note #2 see note 1

Note #3 see note 1

Carl Haber (Lawrence Berkeley Lab.)

There have been delays due to a lack of working FE electronics. We have continued to study dummy modules as means for understanding how to modify the fixtures. Work was done on the hybrid folding problem.

1.1.2.3.2 Development/Prototypes

Milestone	Baseline	Previous	Forecast	Status
Compl Fabr Tools for Proto Mod Assy	14-Jun-99	--	15-Nov-99	Delayed (See #1)
Compl Assy of Proto Modules	29-Nov-99	--	29-Nov-99	On Schedule
Compl Test/Measure Proto Modules	27-Dec-99	--	27-Dec-99	On Schedule

Note #1 Delayed by lack of availability of ICs

Carl Haber (Lawrence Berkeley Lab.)

We have continued to study dummy modules. We believe we can build them

flat now. We have started to prepare components for tests of the ASIC. We learned how to machine the PG sheets and have sent them to CERN for coating. They were received back and have been integrated with BeO facings. A pair of good quality detectors were aligned and glued to a baseboard for use in the ASIC evaluations.

1.1.2.3.3 Production

Carl Haber (Lawrence Berkeley Lab.)

No activity.

1.1.3 Read-Out Drivers

1.1.3.1 Test beam Support

Richard Jared (Lawrence Berkeley Lab.)

Minor support effort was supplied in July.

Andrew Lankford (University Of Calif. At Irvine)

Hardware and software support for laboratory tests of SCT electronics and modules is ongoing. We recently commissioned the last two DSP systems from the last production run. These systems were distributed to collaborators in Japan and the Czech Republic.

1.1.3.2 ROD System Design

1.1.3.2.1 Requirements

Milestone	Baseline	Previous	Forecast	Status
Comp. System design	28-Dec-98	--	28-Dec-98	Completed
System design review	11-Jan-99	--	11-Jan-99	Delayed (See #1)

Note #1 Set for Nov. 15

Richard Jared (Lawrence Berkeley Lab.)

New requirements have been identified that need to be incorporated into the requirements document. It is planned to generate the necessary change control documents next month. None of the additions are expected to have cost or schedule impacts.

1.1.3.2.2 Essential Model

Milestone	Baseline	Previous	Forecast	Status
Compl. SCT Simulation	7-Jul-99	[New]	7-Jul-99	Completed
Complete Pixel ROD Simulation	15-Aug-99	[New]	15-Aug-99	Completed

Richard Jared (Lawrence Berkeley Lab.)

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No refinements of the essential model were made during this period.

1.1.3.2.3 Implementation Model

Milestone	Baseline	Previous	Forecast	Status
Complete system design	28-Dec-98	--	28-Dec-98	Completed
System design review	11-Jan-99	--	11-Jan-99	Delayed (See #1)

Note #1 Set for Nov 15, 1990

Richard Jared (Lawrence Berkeley Lab.)

1.1.3.2.3 ROD Implementation Model (R. Jared)

The architectural definition of the ROD has progressed to the point where the interfaces between FPGAs is the focus of the effort. The simulation of the SCT ROD have been essential to this progress.

1.1.3.3 Design ROD Cards

1.1.3.3.7 Preprototype ROD

Milestone	Baseline	Previous	Forecast	Status
Select implementation approach	30-Oct-98	--	30-Oct-98	Completed (See #1)
Compl PreROD Design	29-Jan-99	29-Jan-99	1-Nov-99	Completed
Compl PreROD Layout	15-Feb-99	15-Feb-99	1-Oct-99	On Schedule
Compl PreROD Procure	1-Mar-99	1-Mar-99	1-Oct-99	On Schedule
Compl PreROD PCB Fab	16-Mar-99	16-Mar-99	15-Oct-99	On Schedule
Compl PreROD Assemble	30-Mar-99	30-Mar-99	1-Nov-99	On Schedule
1st preROD complete	30-Mar-99	30-Mar-99	1-Feb-00	On Schedule
Compl PreROD 2 Debug	6-Aug-99	6-Aug-99	1-Jul-00	On Schedule
Complete Gather VHDL code	1-Oct-99	[New]	1-Oct-99	On Schedule
Complete Decoder VHDL code	1-Oct-99	[New]	1-Oct-99	On Schedule
Compl controller VHDL code	1-Nov-99	[New]	1-Nov-99	On Schedule
compl Mux VHDL code	1-Nov-99	[New]	1-Nov-99	On Schedule
Compl Initial test stand SW	1-Dec-99	[New]	1-Dec-99	On Schedule
Compl DSP C code	1-Dec-99	[New]	1-Dec-99	On Schedule

Note #1 The selection of the implementation approach was time consuming and resulted in a 6-9 month delay to the project. The result was that the preprototype was changed to the prototype ROD. This resulted in being able to maintain the global schedule and recovered some of the costs. The rebase-lining exercise will provide clarity to schedule and cost. The new milestones and forecast dates are intended to provide tracking during the intervening time.

Richard Jared (Lawrence Berkeley Lab.)

Progress has been made on the electronic model, simulation and VHDL code. Simulation of the SCT ROD data path link to link latency has been performed. These simulation show that up to 3 clock link to links latency will satisfy the bandwidth for an occupancy that is 2.5 times the TDR occupancy. Simulation of the pixel RODs is proceeding. The pixel event generator has been coded and tested. The pixel simulation code is now complete. Progress has been made on the VHDL code for the formater FPGA.

1.1.3.4 ROD Prototypes

1.1.3.5 ROD Fabrication

1.1.3.6 ROD Installation